REMARKS

1. Abstract. Corrections are submitted herein above to the Abstract as requested in the Office action, so that the Abstract is 150 words or less.

2. Drawings. Formal Drawings are herein submitted under separate cover as requested in the Office Action.

3. Allowable Claims. Claims 1-18 are pending in the application. The Office action indicated that claims 6, 12 and 18 are allowable if amended so that they are in independent form incorporating all the limitations of the base claims upon which they originally depended. Applicant gratefully acknowledges the Examiner's conclusion and herein submits such amendments so that claims 6, 12 and 18 are now allowable.

4. Claim Rejections. Claims 1-5, 7-11 and 13-17 stand rejected under 35 USC 103(a) as unpatentable over U.S. Patent No. 5,659,716 ("Selvidge"). Applicant herein amends claims 1, 7 and 13 to overcome the rejection.

Attorney discussed the present application with Examiner Pham by telephone on Thursday, May 27, 2004. Attorney explained the reasoning for the amendment to claims 1, 7 and 13, which is also explained herein. Attorney agreed to address, in the present remarks, the matter of what advantage the present invention offers.

The present invention concerns timing of logic operations within a single partition, in one respect. More specifically, claim 1, step d, for example, states that a *pair* of operations in a first domain have a common dependency on a source operation from a second domain. According to the claim, the invention advantageously has an aspect of arranging the first domain so the pair of operations are separated by at least as many operations as the total number of operations in the second domain. This is done because these operations in the first domain compute values successively in response to instances of values from the source operation, and the separating of the pair of operations in the first domain ensures that new instances of the source operation values are computed for each successive one of the instances in which the operations of the first domain compute values depending on the source operation, i.e., "after one value is computed for one instance of an operation depending on a source operation, a next value is computed for the source operation before computing the next

instance of an operation depending on the source operation." Claims 7 and 13 have similar language.

While Selvidge's teachings certainly relate to the general subject of simulation and the timing of logic operations in view of dependencies, the focus of Selvidge is on global links that go into and come out of partitions, and not what goes on within a single partition, except in certain general respects. That is, Selvidge discusses an operation in one partition with regard to it being dependent on multiple global links, i.e., signals from operations from other partitions. See, e.g., Selvidge FIG. 6c and col. 9, lines 3-12 (parent global links d-e_{1-3} and he-$_1$ producing child global link e-f_1).

Also, Selvidge generally recognizes that there is a maximum propagation time through a partition for a critical path in the partition. Selvidge, FIG. 6c and col. 9, lines 16-22 (describing how a child signal from one chip to another is scheduled in response to receipt of parent inter-chip signals the child signal depends upon "after a delay corresponding to the required propagation time for the combinatorial signals of the parents [sic.] to propagate through the logic of the logic partition block 22."). Selvidge appears to be saying in this passage that the partition giving rise to the child signal receives the parent signals at some time t0, that the child's partition has a propagation delay of some time delta_t, and that the child signal is scheduled to be sent no sooner than time t = t0 + delta_t. This is made more clear from what Selvidge says as at col. 13, lines 15-26. That is, in the later passage Selvidge makes it clear that i) the required propagation time through the child's partition, referred to herein as delta_t, is the propagation time for the partition's critical path, i.e., the path having the longest propagation time, ii) the child signal is sent in response to an interconnect clock ("pipeline" clock), and iii) the scheduling of the child signal by a "global router" ensures that this t0 + delta_t constraint is not violated, i.e., that a pipeline clock cycle that occurs after t = t0 + delta_t is chosen for triggering the sending of the child signal.

Selvidge's teachings do not specifically address the same problem to which claims 1, 7 and 13 are directed. The Examiner cites a passage from Selvidge at col. 10, lines 25-32, but this concerns: i) a first operation, g1, in one partition that is dependent on multiple global links parent global links, d-e_{1-3}, ii) a second operation, g2, in the same partition that is dependent on another parent global link, he-$_1$, and iii) the propagation of the results of the operations to

produce child global link e-f_1 in the same partition. Applicant understands, regarding the cited passage from Selvidge, that since gate g2 receives the output of gate g1, therefore gate g2 is in a sense dependent on any global links upon which gate g1 depends. However, this is not what is meant in the teaching and claims of the present invention.

The matter addressed in the present invention claims 1, 7 and 13 concerns timing of two (or more) logic operations within a single domain that receive a result from a third operation from outside their partition. See, for example, FIG. 2 and page 9, lines 1-6 (describing how operation 132 (referred to as operation "o"), operation 130 (referred to as "L130"), and operation 136 (referred to as "L136") in the first domain all receive and depend on operation k from the second domain.)

To make the distinction more clear, Applicant herein amends claims 1, 7 and 13 to state that in the respective domain orderings instances are identified of multiple operations *independently* having dependencies on respective common source operations from other ones of the domains. The reference to "independently having dependencies" refers to situations, such as pointed out immediately above, for example, in which operation 132, operation 130 and operation 136 in the first domain all receive operation k independently from one another so that operation 132, operation 130 and operation 136 all independently have dependencies on operation k.

Although Selvidge shows a gate g2 receiving an output of gate g1, so that gate g2 is in a sense dependent on any global links upon which gate g1 depends, Selvidge does not substantially inform the issue of a pair of operations in the same partition (a first domain) that independently have a common dependency on a source operation from another petition (a second domain). Since Selvidge does not discuss the issue of a pair of operations in the same partition (a first domain) that independently have a common dependency on a source operation from another petition (a second domain), Selvidge, of course, does not teach about arranging the first domain so such a pair of operations are separated by at least as many operations as the total number of operations in the second domain.

Moreover, Selvidge presents no motivation that would even suggest arranging operations within a domain, as claimed in the present invention, since Selvidge teaches that timing dependencies are handled by the scheduling of inter-partition signals (global links), i.e.,

adjusting the timing of an inter-partition signal (by selecting a clock cycle for triggering the sending of the signal) responsive to partition critical paths. *The present invention teaches and claims something akin to the opposite of this*, i.e., adjusting paths in a domain responsive to the timing of inter-domain signals,[1] but with an elegant twist. That is, according to the present invention the time between instances of computing a source operation is not in response to some complicated determination of a critical path within its domain, but rather more elegantly is in response to the total number of operations in the domain of the source operation. Thus, according to the present invention as claimed, the operations of the respective domains are ordered "in second domain orderings, . . . wherein pairs of the operations having the common dependencies are separated by at least as many operations as the total number of operations in the domains of the respective source operations . . ."

The time between instances of computing a source operation is determined by the total number of operations in the domain of the source operation because, according to the present invention, each domain has its own respective ordered sequence of operations, and the operations in each domain are computed simply according to their order in their respective sequence. There is a clock, according to the invention, but it is merely for cycling from one computation to the next, down through the sequences of operations. In this context, there is no selecting of a clock cycle for an operation responsive to a critical path, as in the teachings of Selvidge.

For these reasons, Applicant contends claims 1, 7 and 13, as amended, are patentably distinct over the cited teachings. Claims 2-5, 8-11 and 14-17 are also allowable since they depend on claims 1, 7 and 13, respectively. Moreover, claims 2-5, 8-11 and 14-17 present patentable matter even aside from their dependence upon allowable claims.

The Office action cites teaching by Selvidge about a waiting operation, but this teaching in no way suggests deliberately including a waiting operation between a pair of logical operations in one domain that independently have dependencies on a common source operation from another domain in order to ensure the pair are separated by at least as many operations as

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[1] Selvidge talks in terms of generating signals. In the present invention this is spoken of in terms of values generated by computation of operations.

the total number of operations in the domains of the respective source operations, as claimed in claims 2, 8 and 14 of the present application.

The Office action cites teaching by Selvidge about "ordering" but this teaching in no way suggests a merged ordering of the operations of all the domains, wherein the merged ordering is responsive to the respective domain orderings, as claimed in claims 3, 9 and 15 of the present application. Also compare FIG's 6 and 7 of the present application. All the more certainly, the cited teaching by Selvidge regarding claims 4, 10 and 16 in no way suggests the first merged ordering omits any waiting operations that are in the domain orderings. And even more certainly, the cited teaching by Selvidge regarding claim 5 in no way suggests ordering, in a second merged ordering, the operations of all the domains, wherein the second merged ordering includes separations between pairs of the operations having a common dependency, the separations being of at least the extent as the separations of step d). Claims 11 and 17 have similar language.

PRIOR ART OF RECORD

Applicant has reviewed the prior art of record cited by but not relied upon by Examiner, and assert that the invention is patentably distinct.

REQUESTED ACTION

Applicant contends that the invention as claimed in accordance with amendments submitted herein is patentably distinct, and hereby requests that Examiner grant allowance and prompt passage of the application to issuance.

Respectfully submitted,

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